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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,979	03/11/2004	Jeffery Steven Beck	MICR-161US	6873

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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,979	BECK ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Borg et al. (US 6,476,864).

Regarding claim 1, Borg et al. discloses an active pixel sensor array sampling system comprising:

at least one video circuit (amplifier 230, figure 3A, 4, column 6, lines 17-60) that generates a video voltage from each one of a group of pixels;

at least one reset circuit (amplifier 240 and transistor 330 with reset signal 118, figure 4, column 4, line 3 – column 8, line 12) that generates a reset voltage associated with each one of the pixels in the group of pixels;

wherein one of the at least one video circuit and at least one reset circuit comprises a closed loop sample and hold circuit (figure 4, column 4, lines 20-45).

Regarding claim 2, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a single ended common source amplifier (differential image signal 118, figure 4, column 6, lines 39-60).

Regarding claim 3, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a capacitor (capacitor 78 or 108, figure 4) for holding one of the video voltages and the reset voltages.

Regarding claim 4, Borg et al. discloses wherein the sample and hold circuit includes an amplifier (amplifier 80, figure 4, column 7, lines 10-27) having an input and an output and switches (switches 92, 94, figure 4) that place its capacitor across its input and output.

Regarding claim 5, Borg et al. discloses wherein the pixels are arranged in columns and rows (figure 3A), the at least one video circuit comprises a plurality of video amplifiers (amplifiers 230, figure 3A), each video amplifier being associated with a respective column of pixels, and wherein the at least one reset circuit comprises a plurality of reset amplifiers (amplifier 240, figure 3A), each reset amplifier being associated with one of the video amplifiers.

Regarding claim 6, Borg et al. discloses an active pixel sensor array sampling system comprising:

a video circuit (amplifier 230, figure 3A, 4, column 6, lines 17-60) that generates a video voltage from each one of a group of pixels;

a reset circuit (amplifier 240 and transistor 330 with reset signal 118, figure 4, column 4, line 3 – column 8, line 12) associated with the video circuit that generates a reset voltage associated with each one of the pixels in the group of pixels;

wherein the video circuit and the reset circuit each comprise a closed loop sample and hold circuit (figure 4, column 4, lines 20-45).

Regarding claim 7, Borg et al. discloses wherein the closed loop sample and hold circuit of each of the video circuit and reset circuit comprises a single ended common source amplifier (differential image signal 118, figure 4, column 6, lines 39-60).

Regarding claim 8, Borg et al. discloses wherein the video and reset closed loop sample and hold circuits each comprise a capacitor (capacitor 78 or 108, figure 4) for holding the video voltage and the reset voltage respectively.

Regarding claim 9, Borg et al. discloses wherein each of the sample and hold circuits includes an amplifier (amplifier 80, figure 4, column 7, lines 10-27) having an input and an output and switches (switches 92, 94, figure 4) that place its capacitor across its input and output.

Regarding claim 10, Borg et al. discloses wherein the pixels are arranged in columns and rows and wherein the group of pixels is a column of pixels (group of pixels on each column 38, figure 3A).

Regarding claim 11, Borg et al. discloses a video amplifier (amplifier 230, figure 3A, 4, column 4, lines 15-45); column 6, lines 17-60) for use in sampling an active pixel sensor array

(an active pixel sensor array 280, figure 3A, column 6, lines 17-60), the video amplifier comprising a closed loop sample and hold circuit (figure 4, column 4, lines 15-45).

Regarding claim 12, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a single ended common source amplifier (differential image signal 118, figure 4, column 6, lines 39-60).

Regarding claim 13, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a capacitor (capacitor 78 or 108, figure 4) for holding a video voltage.

Regarding claim 14, Borg et al. discloses wherein the sample and hold circuits further includes an amplifier (amplifier 80, figure 4, column 7, lines 10-27) having an input and an output and switches (switches 92, 94, figure 4) that place the capacitor across the input and output.

Regarding claim 15, Borg et al. discloses an integrated circuit including a video amplifier (amplifier 230, figure 3A, 4, column 4, lines 15-45); column 6, lines 17-60) for use in sampling an active pixel sensor array (an active pixel sensor array 280, figure 3A, column 6, lines 17-60), the video amplifier comprising a closed loop sample and hold circuit (figure 4, column 4, lines 15-45).

Regarding claim 16, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a single ended common source amplifier (differential image signal 118, figure 4, column 6, lines 39-60).

Regarding claim 17, Borg et al. discloses wherein the closed loop sample and hold circuit comprises a capacitor (capacitor 78 or 108, figure 4) for holding a video voltage.

Regarding claim 18, Borg et al. discloses wherein the sample and hold circuits further include an amplifier (amplifier 80, figure 4, column 7, lines 10-27) having an input and an output and switches (switches 92, 94, figure 4) that place the capacitor across the input and output.

Regarding claim 19, Borg et al. discloses wherein the integrated circuit is a CMOS integrated circuit (active pixel sensor array 280, figure 3A, column 1, lines 43-54).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang et al. (US 6,567,028) discloses reference voltage stabilization in CMOS sensors.

Niederkorn et al. (US 6,423,961) discloses pixel readout switched capacitor buffer circuit and method therefor.

Sohn (US 6,365,950) discloses CMOS active pixel sensor.

Kokubun (US 7,113,215) discloses CMOS image sensor.

Barna (US 2004/0036783) discloses asymmetric comparator for use in pixel oversaturation detection.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LN
4/13/07

LUONG T. NGUYEN
PATENT EXAMINER